

De 1 13. (Original) The device of claim ¹/~~9~~ wherein the thickness of the CES layer is
2 smaller than 600Å.

1 14. (Withdrawn - Currently Amended) A method for fabricating at least one
2 semiconductor device having a gate region and recessed spacers, comprising:

3 forming a substrate;

4 forming a gate region on top of the substrate, the gate region having a gate
5 electrode and a gate dielectric region;

6 forming ~~two~~ a sidewall liner along a side of ~~liners~~ confining the gate region
7 ~~therebetween~~;

8 forming ~~a two-spacers~~ spacer on top of the sidewall ~~liners~~ liner ~~on both sides of~~
9 ~~the gate region~~, a height of the ~~spacers~~ spacer matching substantially a height of the
10 sidewall ~~spacers~~ liner;

11 reducing the width of the sidewall ~~liners~~ liner underneath the ~~spacers~~ spacer to
12 pull back from an edge of each spacer by a predetermined distance; and

13 forming ~~two~~ a recessed ~~spacers~~ spacer by reducing the height of the formed
14 ~~spacers~~ spacer, wherein the reduced spacer height reduces device channel stress.

1 15. (Withdrawn - Currently Amended) The method of claim 14 wherein the
2 forming ~~two-spacers~~ a spacer further includes depositing spacer material and etching
3 the deposited spacer material so that the top of the spacer slopes ~~spacers~~ slope down
4 from the top of the sidewall ~~liners~~ liner to a horizontal part of the sidewall liner that
5 extends along the substrate from the gate region.